CLAIMS:

What is claimed is:

1. A DRAM cell comprising:

a semiconductor substrate;

a trench extending into the substrate;

a cell capacitor disposed in a bottom portion of the trench;

a cell transistor disposed in a top portion of the trench above the cell capacitor;

a node conducting element connecting the cell capacitor to the cell transistor; and

a collar disposed about the node conducting element between the cell transistor and the cell capacitor;

wherein:

the collar is disposed in the substrate, at least partially outside of the trench, between the cell capacitor and the cell transistor.

2. A DRAM cell, according to claim 1, wherein:

the collar is disposed substantially outside of the trench.

3. A DRAM cell, according to claim 1, wherein:

the collar is disposed wholly outside of the trench

4. A DRAM cell, according to claim 1, further comprising:

a strap disposed between the node conducting element and the cell transistor.

5. A DRAM cell, according to claim 1, further comprising:

a strap which is self-aligned with the collar.

6. A DRAM cell, according to claim 1, further comprising:
a strap disposed in the trench at substantially a same depth as the collar.

7. A DRAM cell, according to claim 1, further comprising:
a strap disposed in the trench and laterally surrounded by the collar.

8. A DRAM cell, according to claim 1, further comprising:
a strap disposed in the trench and having a periphery; and
the collar is laterally adjacent and surrounds the periphery of the buried strap.

9. A DRAM cell comprising:
a semiconductor substrate;
a trench extending into the substrate;
a cell capacitor disposed in a bottom portion of the trench;
a cell transistor disposed in a top portion of the trench above the cell capacitor;
a node conducting element connecting the cell capacitor to the cell transistor; and
a collar disposed about the node conducting element between the cell transistor and the cell capacitor; and
a strap;
wherein:
the strap is embedded into a top surface of the collar.

10. A DRAM cell, according to claim 9, wherein:
the strap extends no higher than the collar.

11. A DRAM cell, according to claim 9, wherein:
the strap is has a periphery which is laterally surrounded by the collar.

12. A method of forming DRAM cells, comprising:
forming trenches in a semiconductor substrate;
forming cell capacitors in a bottom portion of the trench;
forming cell transistors in a top portion of the trench; and
for each DRAM cell, providing a collar between the cell capacitor and the cell transistor, the collar being disposed in the substrate, at least partially outside of the trench.

13. A method, according to claim 12, wherein:
the collar is disposed substantially outside of the trench.

14. A method, according to claim 12, wherein:
the collar is disposed wholly outside of the trench

15. A method, according to claim 12, further comprising:
for each DRAM cell, providing a node conducting element between the cell capacitor and the cell transistor;
wherein:
the collar is disposed laterally adjacent the node poly element.

16. A method, according to claim 12, further comprising:

for each DRAM cell, providing a node conducting element between the cell capacitor and the cell transistor;

wherein:

the collar surrounds a periphery of the node poly element.

17. A method, according to claim 12, further comprising:

for each DRAM cell, providing a node conducting element between the cell capacitor and the cell transistor; and

a strap disposed between the node conducting element and the cell transistor.

18. A method, according to claim 12, further comprising:

for each DRAM cell, providing a strap which is self-aligned with the collar.

19. A method, according to claim 12, further comprising:

for each DRAM cell, disposing a strap in the trench at substantially a same depth as the collar.

20. A method, according to claim 12, further comprising:

for each DRAM cell, disposing a strap in the trench; and

the strap is laterally surrounded by the collar.